CLAIMS

1. A method for debugging an electronic system having instrumentation circuitry included therein, wherein the electronic system is described with an HDL, said method comprising:

(a) activating certain design visibility, design patching or design control aspects of the instrumentation circuitry available for examining or modifying the electronic system via the instrumentation circuitry;

(b) determining configuration information based on the certain design visibility, design patching or design control aspects that are activated;

(c) configuring the instrumentation circuitry in accordance with the configuration information;

(d) receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product;

(e) translating the debug data into HDL-related debug information; and

(f) relating the HDL-related debug information to the HDL description.

2. A method as recited in claim 1, wherein the HDL description is a high-level HDL description.

3. A method as recited in claim 2, wherein the HDL-related debug information is described in a high-level HDL.

4. A method as recited in claim 1, wherein said translating (e) is performed automatically.

5. A method as recited in claim 1, wherein said method operates without any requirement for a test bench.

6. A method as recited in claim 1, wherein the debug data includes at least status information or sampling data.

7. A method as recited in claim 1, wherein said activating (a) operates to enable a user to activate the certain design visibility, design patching or design control aspects.

8. A method as recited in claim 7, wherein said activating (a) is performed using a graphical user interface.

9. A method as recited in claim 1, wherein said method further comprises:

(g) displaying the high-level HDL description with the HDL-related debug information related thereto.

10. A method as recited in claim 1, wherein the design control aspects include trigger conditions, and wherein said activating (a) operates to enable a user to set one or more trigger conditions from the trigger conditions available by the instrumentation circuitry.

11. A method as recited in claim 1, wherein the electronic system comprises an integrated circuit.

12. A method as recited in claim 1, wherein the electronic system comprises a programmable integrated circuit.

13. A method as recited in claim 1, wherein the electronic system includes a hardware portion and a software portion, and

wherein said method further comprises:

(g) interacting with a software debugger which debugs the software of the electronic system.

14. A method as recited in claim 1, wherein said method further comprises:

(g) interacting with a functional simulator which simulates a portion of the electronic system.

15. A method as recited in claim 1, wherein the electronic system is operated in its target environment and running at its target speed during said debugging.

16. A method as recited in claim 14, wherein the target environment includes real-time characteristics.

17. A method as recited in claim 1, wherein while debugging the electronic system, the electronic system is operating in its target environment without interruption for the purpose of debugging.

18. A method as recited in claim 1, wherein said debugging operates to identify at least one fault of the electronic system.

19. A method as recited in claim 18, wherein the at least one fault is selected from the group consisting of: specification error, design error, tool error, device driver error, timing error, manufacturing fault, and environment error,

20. A method as recited in claim 1, wherein the instrumentation circuitry comprises design instrumentation circuitry.

21. A method for debugging an integrated circuit product having instrumentation circuitry included therein, wherein the integrated circuit product was designed with a high-level HDL description, said method comprising:

(a) activating certain aspects available for examining or modifying by the instrumentation circuitry;

(b) determining configuration information based on the certain aspects that are activated;

(c) configuring the instrumentation circuitry in accordance with the configuration information;

(d) receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product;

(e) translating the debug data into HDL-related debug information;

(f) relating the HDL-related debug information to the high-level HDL description;

(g) thereafter retrieving circuit status information for the integrated circuit product via the instrumentation circuitry;

(h) displaying state information concerning the integrated circuit product based on the retrieved circuit status information.

22. A method as recited in claim 21, wherein the HDL-related debug information is described in a high-level HDL.

23. A method as recited in claim 21, wherein said displaying (h) comprises:

relating the state information to the high-level HDL description; and

displaying the high-level HDL description of the integrated circuit product with the state information related thereto.

24. A method as recited in claim 21,

wherein the state information includes signal values for signals, and

wherein said relating operates to relate the signal values to HDL identifiers within the high-level HDL description that correspond to the signals.